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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,847	01/05/2006	Adrianus Sempel	GB 030106	5407

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EXAMINER	
WILLIS, RANDAL L	
ART UNIT	**PAPER NUMBER**
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,847	SEMPEL ET AL.	
	Examiner	Art Unit	
	RANDAL WILLIS	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/8/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/563847 filed January 5th 2006. Claims 1-17 are currently pending and have been examined.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 3/08/2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

5. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the

Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-4, 6, 8-13, 15-17 rejected under 35 U.S.C. 102(e) as being anticipated by Kimura (2004/0085270).

Apropos claim 1, Kimura teaches:

A display device comprising:

a matrix array of display elements (pixels of display in pixel portion 402, Fig. 11a) each driven by an input provided on a data conductor (Signal Lines Si, Fig. 4); and

data conductor addressing circuitry (Data driver 419, Fig. 4) for generating the inputs in response to input data, wherein the data conductor addressing circuitry comprises:

a plurality of controllable driver circuits (driver circuits 437 and 438, Fig. 4), each for providing an input to an associated data conductor (driver circuits provide signal line Si output, Fig. 4), wherein the number of controllable driver circuits is at least one greater than the number required for providing data to all data conductors (See Fig. 4, 2 driver circuits for each signal line); and

a reference driver circuit (109, Fig. 4), wherein the reference driver circuit is for calibrating at least one of the controllable driver circuits whilst the other controllable driver circuits provide inputs to the data conductors (109 sets the current for one of 437 or 438 while the other circuit is providing the output to Si, [0212]).

Apropos claim 2, Kimura teaches:

A device as claimed in claim 1, comprising a matrix array of current-addressed display elements (pixels of pixel portion 402, Fig. 11a), each driven by an input current, and wherein the driver circuits (437 and 438, Fig. 4) comprise current source circuits (See current source circuits in Fig. 4) for providing an input current to the associated data conductor (Current output to signal lines Si, Fig. 4), and the reference driver circuit comprises a reference current source (See current source in 109, Fig. 4).

Apropos claim 3, Kimura teaches:

A device as claimed in claim 2, wherein each display element is provided with an associated switching circuit (Switching TFT 503, Fig. 16A) for sampling the input current and subsequently providing the sampled input current to the display element (506, Fig. 16A).

Apropos claim 4, Kimura teaches:

A device as claimed in claim 3, comprising an active matrix electroluminescent display device (light emitting display, [0001]).

Apropos claim 6, Kimura teaches:

A device as claimed in claim 1, wherein the number of driver circuits (32,34,40) required for providing inputs to all data conductors (6) is equal to the number of data conductors (Every signal line Si receives input from one driver circuit, either 437 or 438 during driving [0212]).

Apropos claim 8, Kimura teaches:

A device as claimed in claim 4, wherein the number of current source circuits required for providing currents to all data conductors is equal to a multiple of the number of data conductors, and wherein the current for each data conductor is provided by the multiple number of current source circuits (Kimura teaches that each of the current sources can be made of a plurality of current sources as shown in Fig. 18A).

Apropos claim 9, Kimura teaches:

A device as claimed in claim 8, wherein the multiple number of current source circuits (60) providing current to an associated data conductor is selected from a group (current sources 555-558, Fig. 18A) having a larger number of current source circuits, and the multiple number is formed from a different selection from the group at different times (Different sources selected based on signal [0021]).

Apropos claim 10, Kimura teaches:

A device as claimed in claim 1, wherein the reference driver circuit is for calibrating each of the controllable driver circuits in a sequence (Calibrates 437, then 438, Fig. 4), and wherein the controllable driver circuits not being calibrated together provide the inputs to all data conductors (Switches are inversely connected, so when one is being set by 109, the other is providing input to the signal lines [0212]).

Apropos claim 11, Kimura teaches:

A method of providing drive signals to the data conductors (Si, Fig. 4) of a display device during a data addressing period (Data supplied during setting operation, which is the same as addressing period [0212]), the display device comprising an array of display elements (402, Fig. 11a), the method comprising:

generating inputs to be provided to the data conductors in response to input data using a plurality of controllable driver circuits (437 Fig. 4) selected from a number of

controllable driver circuits which is at least one greater than the number required for providing inputs to all data conductors (437 and 438, Fig. 4);

simultaneously calibrating the remaining at least one further controllable driver circuit using a reference driver circuit (Sets one of the driver circuits 437 or 438 with 109 while driving Si with the other, Fig. 4 [0212]), wherein a different driver circuit or circuits are calibrated during different data addressing periods (switch 439 switches the operation of the two circuits, Fig. 4).

Apropos claim 12, Kimura teaches:

A method as claimed in claim 11 for providing current drive signals to the data conductors, the display device comprising an array of current-addressed display elements (402, Fig. 11a), the controllable driver circuits (437, 438 Fig. 4) comprising controllable current source circuits (See current sources in Fig. 4) and the reference driver circuit comprising a reference current source (109, Fig. 4), and wherein the method comprises generating input currents in response to the input data (Si currents derived from Video Data, Fig. 4).

Apropos claim 13, Kimura teaches:

A method as claimed in claim 11 wherein one driver circuit is used to provide the input to each data conductor (Si supplied current from only one of 437 or 438 at any one time).

Apropos claim 15, Kimura teaches:

A method as claimed in claim 12, wherein a plurality of current source circuits is used to provide the input current to each data conductor (current sources 555-558, Fig. 18A [0021]).

Apropos claim 16, Kimura teaches:

A method as claimed in claim 15, wherein the plurality of current source circuits (60) providing the input current to each data conductor is selected from a group (current sources 555-558, Fig. 18A) having a larger number of current source circuits, and the multiple number is formed from a different selection from the group at different times (Different sources selected based on signal [0021]).

Apropos claim 17, Kimura teaches:

A method as claimed in 11, wherein the reference driver circuit is used to calibrate each of the controllable driver circuits in a sequence (Calibrates 437, then 438, Fig. 4), and wherein the controllable driver circuits not being calibrated together provide the inputs to all data conductors (Switches are inversely connected, so when one is being set by 109, the other is providing input to the signal lines [0212]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 5, 7 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (2004/0085270).

Apropos claim 5, Kimura teaches:

A device as claimed in claim 1, comprising a matrix array of addressed display elements (pixels of pixel portion 402, Fig. 11a), each driven by an input, and wherein the driver circuits (437 and 438, Fig. 4) comprise source circuits (See current source circuits in Fig. 4) for providing an input to the associated data conductor (Current output to signal lines Si, Fig. 4), and the reference driver circuit comprises a reference source (See current source in 109, Fig. 4).

However, Kimura fails to explicitly teach voltage-addressed display elements and driving them with voltage sources.

Examiner takes official notice that one of ordinary skill in the art at the time of the invention could simply replace the current sources of Kimura for voltage sources without

disturbing the inventive concept of Kimura in order to apply the reduction of variations in TFTs that Kimura provides ([0055]) in a voltage driven display device.

Apropos claim 7 and 14, Kimura fails to explicitly teach

wherein the number of driver circuits (32,34,40) required for providing inputs to all data conductors is equal to a fraction of the number of data conductors, and wherein each driver circuit is for providing inputs to a group of data conductors in multiplexed manner.

However, Examiner takes official notice that the use of multiplexers in order to route the output of a single driver circuit to the buffers of multiple data lines is well known in the art and therefore would have been obvious to one of ordinary skill in the art at the time of the invention in order to save room in the driver IC.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yun (7,259,739) for teaching multiplexing data to data latches.

Lambert (6,816,143) for teaching one driver more than required in order to prevent defects.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RANDAL WILLIS whose telephone number is (571)270-

1461. The examiner can normally be reached on Monday to Thursday, 8am to 5pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RLW

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629